7-2 EDGE-TRIGGERED FLIP-FLOPS

Flip-flops are synchronous bistable devices, also known as *bistable multivibrators*. In this case, the term *synchronous* means that the output changes state only at a specified point on a triggering input called the *clock* (CLK), which is designated as a control input, *C*; that is, changes in the output occur in synchronization with the clock.

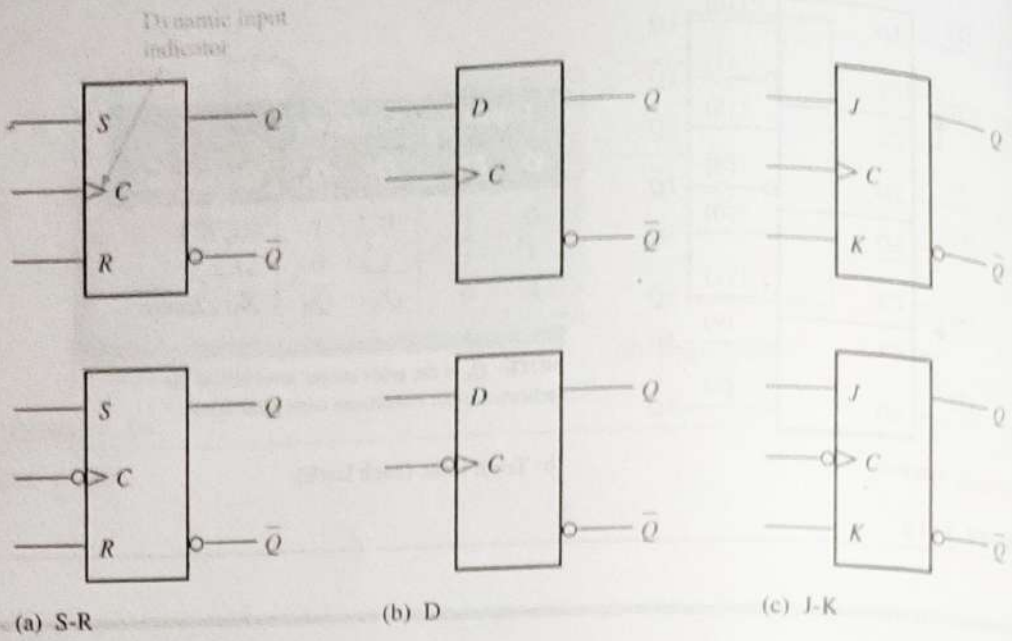
After completing this section, you should be able to

- Define *clock*
- Define *edge-triggered flip-flop*
- Explain the difference between a flip-flop and a latch
- Identify an edge-triggered flip-flop by its logic symbol
- Discuss the difference between a positive and a negative edge-triggered flip-flop
- Discuss and compare the operation of S-R, D, and J-K edge-triggered flip-flops and explain the differences in their truth tables
- Discuss the asynchronous inputs of a flip-flop
- Describe the 74AHC74 and the 74HC112 flip-flops

An **edge-triggered flip-flop** changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock. Three types of edge-triggered flip-flops are covered in this section: S-R, D, and J-K. Although the S-R flip-flop is not available in IC form, it is the basis for the D and J-K flip-flops and is, therefore, important to cover. The logic symbols for all of these flip-flops are shown in Figure 7–13. Notice that each type can be either positive edge-triggered (no bubble at *C* input) or negative edge-triggered (bubble at *C* input). The key to identifying an edge-triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (*C*) input. This triangle is called the *dynamic input indicator* ▷.

► FIGURE 7–13

Edge-triggered flip-flop logic symbols

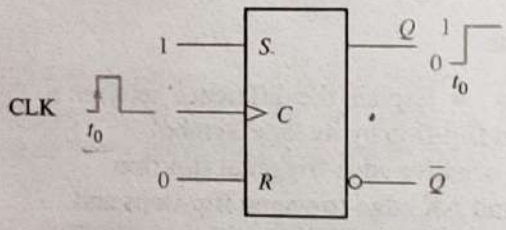


The Edge-Triggered S-R Flip-Flop

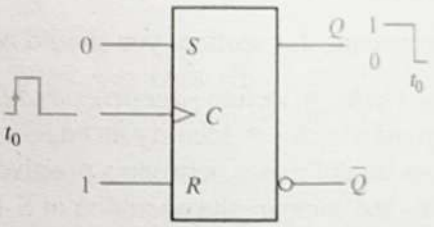
An S-R flip-flop cannot have both *S* and *R* inputs HIGH at the same time.

The *S* and *R* inputs of the **S-R flip-flop** are called **synchronous** inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse. When *S* is HIGH and *R* is LOW, the *Q* output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET. When *S* is LOW and *R* is HIGH, the *Q* output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET. When both *S* and *R* are LOW, the output does not change from its prior state. An invalid condition exists when both *S* and *R* are HIGH.

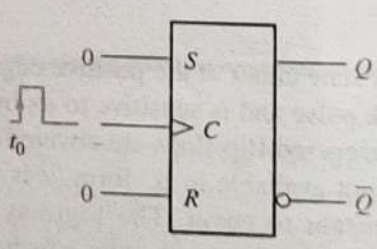
This basic operation of a positive edge-triggered flip-flop is illustrated in Figure 7–14, and Table 7–2 is the truth table for this type of flip-flop. Remember, *the flip-flop cannot change state except on the triggering edge of a clock pulse*. The *S* and *R* inputs can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output.



(a) $S = 1$, $R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0$, $R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

▲ FIGURE 7–14

Operation of a positive edge-triggered S-R flip-flop

TABLE 7–2
Truth table for a positive edge-triggered S-R flip-flop

INPUTS S	R	CLK	OUTPUTS Q	$\overline{Q}$	COMMENTS
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

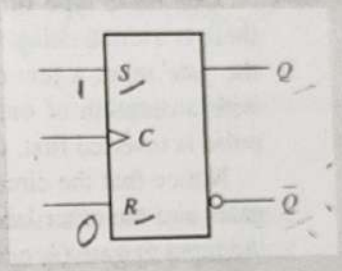
↑ = clock transition LOW to HIGH
X = irrelevant ("don't care")
Q_0 = output level prior to clock transition

The operation and truth table for a negative edge-triggered S-R flip-flop are the same as those for a positive edge-triggered device except that the falling edge of the clock pulse is the triggering edge.

EXAMPLE 7–4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure 7–15 for the S, R, and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

FIGURE 7–15



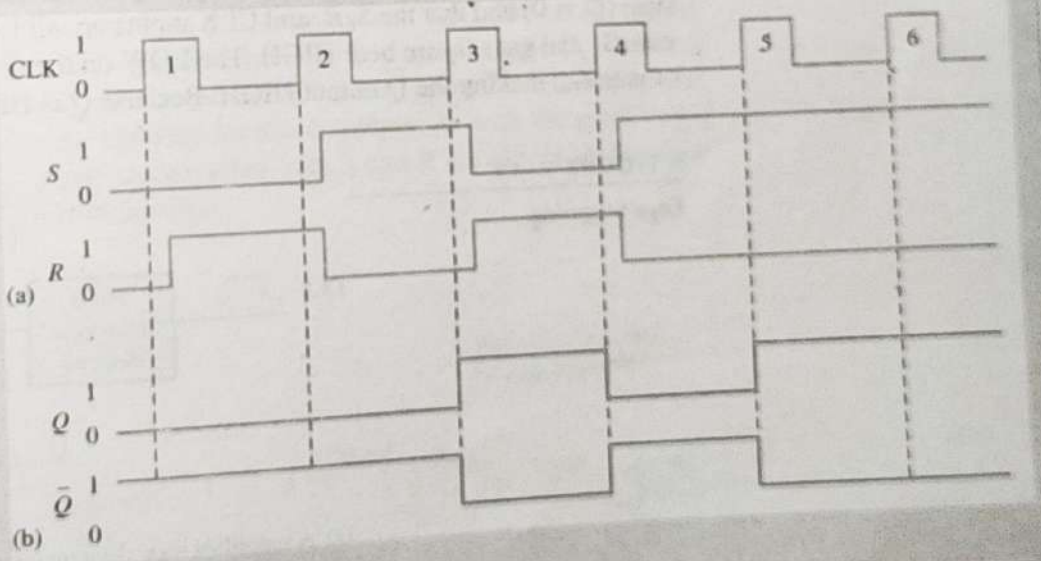


FIGURE 7–16

Solution

1. At clock pulse 1, S is LOW and R is LOW, so Q does not change.
2. At clock pulse 2, S is LOW and R is HIGH, so Q remains LOW (RESET).
3. At clock pulse 3, S is HIGH and R is LOW, so Q goes HIGH (SET).

4. At clock pulse 4, S is LOW and R is HIGH, so Q goes LOW (RESET).
5. At clock pulse 5, S is HIGH and R is LOW, so Q goes HIGH (SET).
6. At clock pulse 6, S is HIGH and R is LOW, so Q stays HIGH.

Once Q is determined, $\overline{Q}$ is easily found since it is simply the complement of Q. The resulting waveforms for Q and $\overline{Q}$ are shown in Figure 7–16(b) for the input waveforms in part (a).

Supplementary Problem Determine Q and $\overline{Q}$ for the S and R inputs in Figure 7–16(a) if the flip-flop is a negative edge-triggered device.

A Method of Edge-Triggering

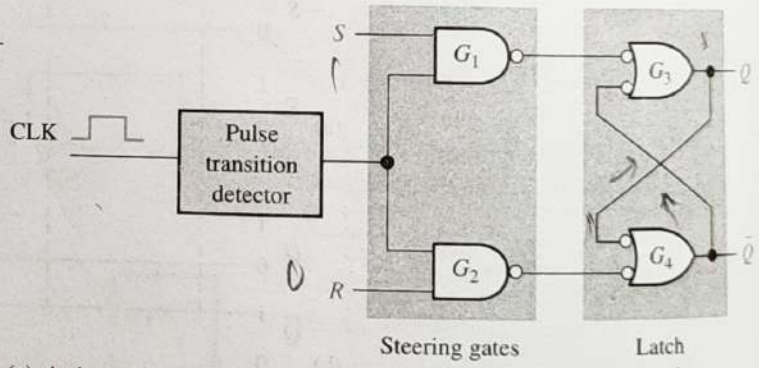
A simplified implementation of an edge-triggered S-R flip-flop is illustrated in Figure 7–17(a) and is used to demonstrate the concept of edge-triggering. This coverage of the S-R flip-flop does not imply that it is the most important type. Actually, the D flip-flop and the J-K flip-flop are available in IC form and more widely used than the S-R type. However, understanding the S-R is important because both the D and the J-K flip-flops are derived from the S-R flip-flop. Notice that the S-R flip-flop differs from the gated S-R latch only in that it has a pulse transition detector. This circuit produces a very short-duration spike on the positive-going transition of the clock pulse.

One basic type of pulse transition detector is shown in Figure 7–17(b). As you can see, there is a small delay on one input to the NAND gate so that the inverted clock pulse arrives at the gate input a few nanoseconds after the true clock pulse. This produces an output spike with a duration of only a few nanoseconds. In a negative edge-triggered flip-flop the clock pulse is inverted first, thus producing a narrow spike on the negative-going edge.

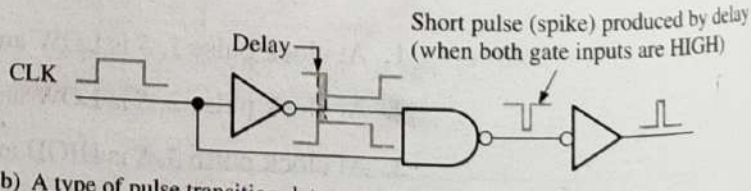
Notice that the circuit in Figure 7–17 is partitioned into two sections, one labeled Steering gates and the other labeled Latch. The steering gates direct, or steer, the clock spike either to the input to gate G_3 or to the input to gate G_4, depending on the state of the S and R inputs. To understand the operation of this flip-flop, begin with the assumptions that it is in the RESET state ($Q = 0$) and that the S, R, and CLK inputs are all LOW. For this condition, the outputs of gate G_1 and gate G_2 are both HIGH. The LOW on the Q output is coupled back into one input of gate G_4, making the $\overline{Q}$ output HIGH. Because $\overline{Q}$ is HIGH, both inputs to gate G_3 are HIGH

▶ **FIGURE 7–17**

Edge triggering



(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

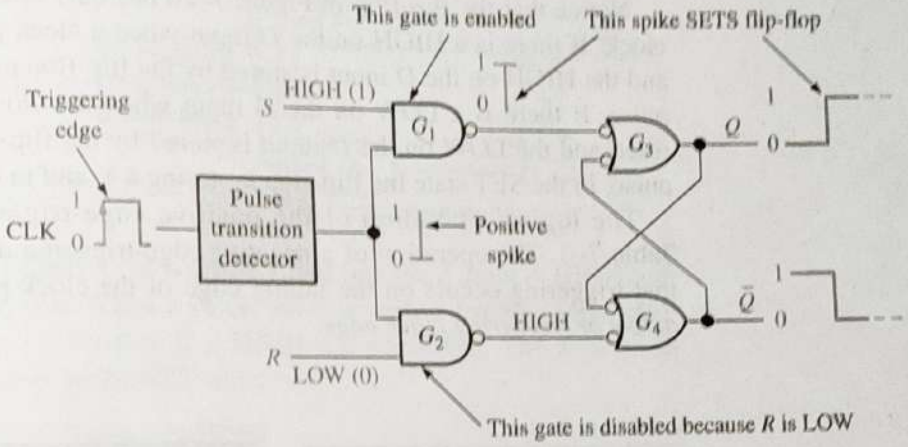


(b) A type of pulse transition detector

(remember, the output of gate G_1 is HIGH), holding the Q output LOW. If a pulse is applied to the CLK input, the outputs of gates G_1 and G_2 remain HIGH because they are disabled by the LOWs on the S input and the R input; therefore, there is no change in the state of the flip-flop—it remains in the RESET state.

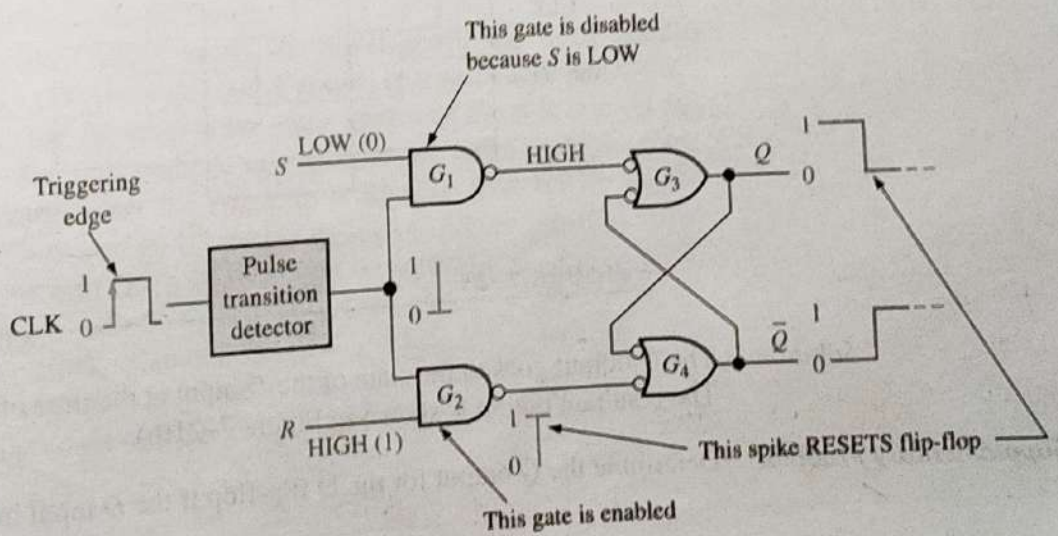
Let us now make S HIGH, leave R LOW, and apply a clock pulse. Because the S input to gate G_1 is now HIGH, the output of gate G_1 goes LOW for a very short time (spike) when CLK goes HIGH, causing the Q output to go HIGH. Both inputs to gate G_4 are now HIGH (remember, gate G_2 output is HIGH because R is LOW), forcing the $\overline{Q}$ output LOW. This LOW on $\overline{Q}$ is coupled back into one input of gate G_3, ensuring that the Q output will remain HIGH. The flip-flop is now in the SET state. Figure 7–18 illustrates the logic level transitions that take place within the flip-flop for this condition.

▶ FIGURE 7–18



Next, let us make S LOW and R HIGH and apply a clock pulse. Because the R input is now HIGH, the positive-going edge of the clock produces a negative-going spike on the output of gate G_2, causing the $\overline{Q}$ output to go HIGH. Because of this HIGH on $\overline{Q}$, both inputs to gate G_3 are now HIGH (remember, the output of gate G_1 is HIGH because of the LOW on S), forcing the Q output to go LOW. This LOW on Q is coupled back into one input of gate G_4, ensuring that $\overline{Q}$ will remain HIGH. The flip-flop is now in the RESET state. Figure 7–19 illustrates the logic level transitions that occur within the flip-flop for this condition. As with the gated latch, an invalid condition exists if a clock pulse occurs when both S and R are HIGH at the same time. This is the major drawback of the S-R flip-flop.

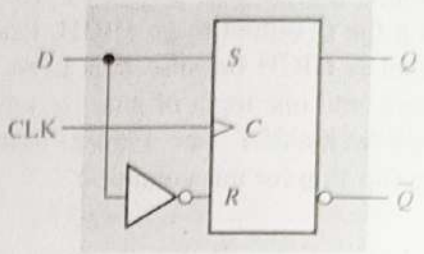
▶ FIGURE 7–19



The Edge-Triggered D Flip-Flop

The **D flip-flop** is useful when a single data bit (1 or 0) is to be stored. The addition of an inverter to an S-R flip-flop creates a basic D flip-flop, as in Figure 7–20, where a positive edge-triggered type is shown.

▶ **FIGURE 7–20**



Notice that the flip-flop in Figure 7–20 has only one input, the *D* input, in addition to the clock. If there is a HIGH on the *D* input when a clock pulse is applied, the flip-flop will set, and the HIGH on the *D* input is stored by the flip-flop on the positive-going edge of the clock pulse. If there is a LOW on the *D* input when the clock pulse is applied, the flip-flop will reset, and the LOW on the *D* input is stored by the flip-flop on the leading edge of the clock pulse. In the SET state the flip-flop is storing a 1, and in the RESET state it is storing a 0.

The logical operation of the positive edge-triggered D flip-flop is summarized in Table 7–3. The operation of a negative edge-triggered device is, of course, the same, except that triggering occurs on the falling edge of the clock pulse. *Remember, Q follows D at the active or triggering clock edge.*

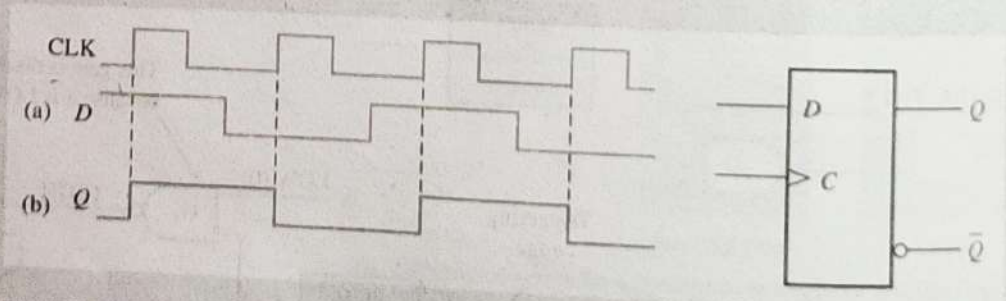
▶ **TABLE 7–3**

INPUTS		OUTPUTS		
D	CLK	*Q*	$\overline{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

EXAMPLE 7–5

Given the waveforms in Figure 7–21(a) for the *D* input and the clock, determine the *Q* output waveform if the flip-flop starts out RESET.



▲ **FIGURE 7–21**

Solution The *Q* output goes to the state of the *D* input at the time of the positive-going clock edge. The resultant output is shown in Figure 7–21(b).

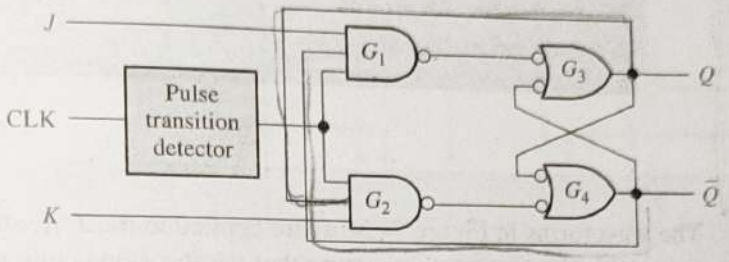
Supplementary Problem Determine the *Q* output for the D flip-flop if the *D* input in Figure 7–21(a) is inverted.

The Edge-Triggered J-K Flip-Flop

The **J-K flip-flop** is versatile and is a widely used type of flip-flop. The J and K designations for the inputs have no known significance except that they are adjacent letters in the alphabet. The functioning of the J-K flip-flop is identical to that of the S-R flip-flop in the SET, RESET, and no-change conditions of operation. *The difference is that the J-K flip-flop has no invalid state as does the S-R flip-flop.*

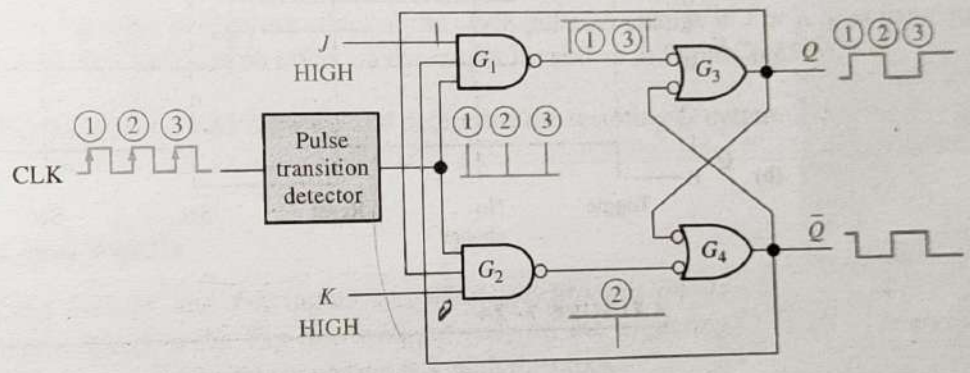
Figure 7–22 shows the basic internal logic for a positive edge-triggered J-K flip-flop. Notice that it differs from the S-R edge-triggered flip-flop in that the Q output is connected back to the input of gate G_2, and the $\overline{Q}$ output is connected back to the input of gate G_1. The two inputs are labeled J and K. A J-K flip-flop can also be of the negative edge-triggered type, in which case the clock input is inverted.

▶ FIGURE 7–22



Let us assume that the flip-flop in Figure 7–23 is RESET and that the J input is HIGH and the K input is LOW rather than as shown. When a clock pulse occurs, a leading-edge spike indicated by ① is passed through gate G_1 because $\overline{Q}$ is HIGH and J is HIGH. This will cause the latch portion of the flip-flop to change to the SET state.

▶ FIGURE 7–23



The flip-flop is now SET. If you now make J LOW and K HIGH, the next clock spike indicated by ② will pass through gate G_2 because Q is HIGH and K is HIGH. This will cause the latch portion of the flip-flop to change to the RESET state.

Now, if a LOW is applied to both the J and K inputs, the flip-flop will stay in its present state when a clock pulse occurs. So, a LOW on both J and K results in a *no-change* condition.

So far, the logical operation of the J-K flip-flop is the same as that of the S-R type in the SET, RESET, and no-change modes. The difference in operation occurs when both the J and K inputs are HIGH. To see this, assume that the flip-flop is RESET. The HIGH on the $\overline{Q}$ enables gate G_1, so the clock spike indicated by ③ passes through to set the flip-flop. Now, there is a HIGH on Q, which allows the next clock spike to pass through gate G_2 and reset the flip-flop.

As you can see, on each successive clock spike, the flip-flop changes to the opposite state. This mode is called **toggle** operation. Figure 7–23 illustrates the transitions when the flip-flop is in the toggle mode. A J-K flip-flop connected for toggle operation is sometimes called a *T flip-flop*.

Table 7–4 summarizes the logical operation of the edge-triggered J-K flip-flop in truth table form. *Notice that there is no invalid state as there is with an S-R flip-flop.* The truth table for a negative edge-triggered device is identical except that it is triggered on the falling edge of the clock pulse.

TABLE 7–4

Truth table for a positive edge-triggered J-K flip-flop

INPUTS			OUTPUTS		COMMENTS
J	K	CLK	Q	$\overline{Q}$	
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

EXAMPLE 7–6

The waveforms in Figure 7–24(a) are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.

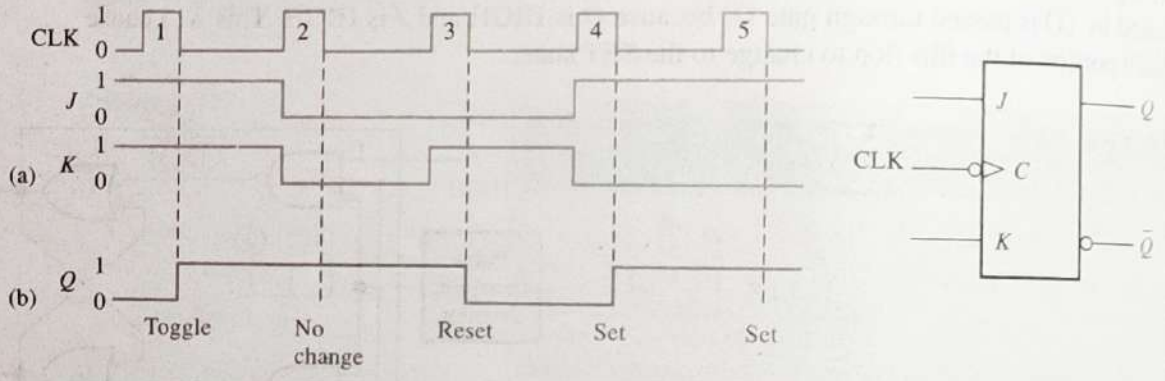


FIGURE 7–24

Solution

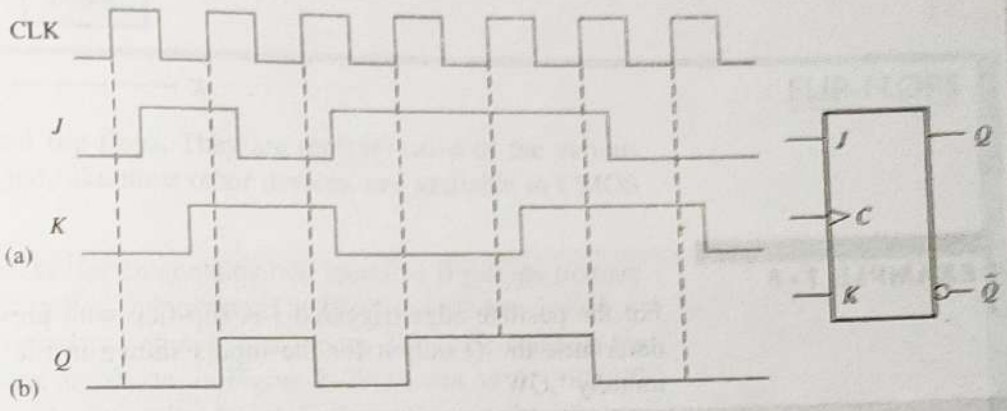
1. First, since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the Q output will change only on the negative-going edge of the clock pulse.
2. At the first clock pulse, both J and K are HIGH; and because this is a toggle condition, Q goes HIGH.
3. At clock pulse 2, a no-change condition exists on the inputs, keeping Q at a HIGH level.
4. When clock pulse 3 occurs, J is LOW and K is HIGH, resulting in a RESET condition; Q goes LOW.
5. At clock pulse 4, J is HIGH and K is LOW, resulting in a SET condition; Q goes HIGH.
6. A SET condition still exists on J and K when clock pulse 5 occurs, so Q will remain HIGH.

The resulting Q wavefcrm is indicated in Figure 7–24(b).

Supplementary Problem Determine the Q output of the J-K flip-flop if the J and K inputs in Figure 7–24(a) are inverted.

EXAMPLE 7–7

The waveforms in Figure 7–25(a) are applied to the flip-flop as shown. Determine the Q output, starting in the RESET state.



▲ **FIGURE 7–25**

Solution The Q output assumes the state determined by the states of the J and K inputs at the positive-going edge (triggering edge) of the clock pulse. A change in J or K after the triggering edge of the clock has no effect on the output, as shown in Figure 7–25(b).

Supplementary Problem Interchange the J and K inputs and determine the resulting Q output.

Asynchronous Preset and Clear Inputs

For the flip-flops just discussed, the S-R, D, and J-K inputs are called *synchronous inputs* because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse; that is, the data are transferred synchronously with the clock.

Most integrated circuit flip-flops also have **asynchronous** inputs. These are inputs that affect the state of the flip-flop *independent of the clock*. They are normally labeled **preset** (*PRE*) and **clear** (*CLR*), or *direct set* (S_D) and *direct reset* (R_D) by some manufacturers. An active level on the preset input will set the flip-flop, and an active level on the clear input will reset it. A logic symbol for a J-K flip-flop with preset and clear inputs is shown in Figure 7–26. These inputs are active-LOW, as indicated by the bubbles. These preset and clear inputs must both be kept HIGH for synchronous operation.

▶ **FIGURE 7–26**

Logic symbol for a J-K flip-flop with active-LOW preset and clear inputs

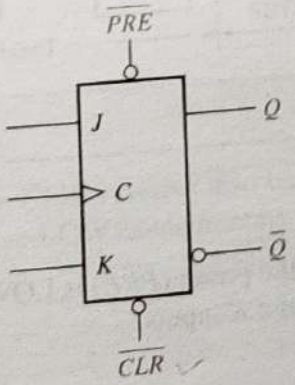
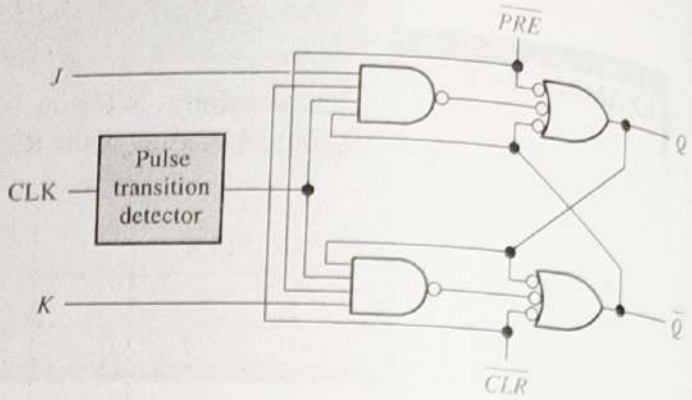


Figure 7–27 shows the logic diagram for an edge-triggered J-K flip-flop with active-LOW preset ($\overline{PRE}$) and clear ($\overline{CLR}$) inputs. This figure illustrates basically how these inputs work. As you can see, they are connected so that they override the effect of the synchronous inputs, *J*, *K*, and the clock.

FIGURE 7–27

Logic diagram for a basic J-K flip-flop with active-LOW preset and clear inputs



EXAMPLE 7–8

For the positive edge-triggered J-K flip-flop with preset and clear inputs in Figure 7–28, determine the *Q* output for the inputs shown in the timing diagram in part (a) if *Q* is initially LOW.

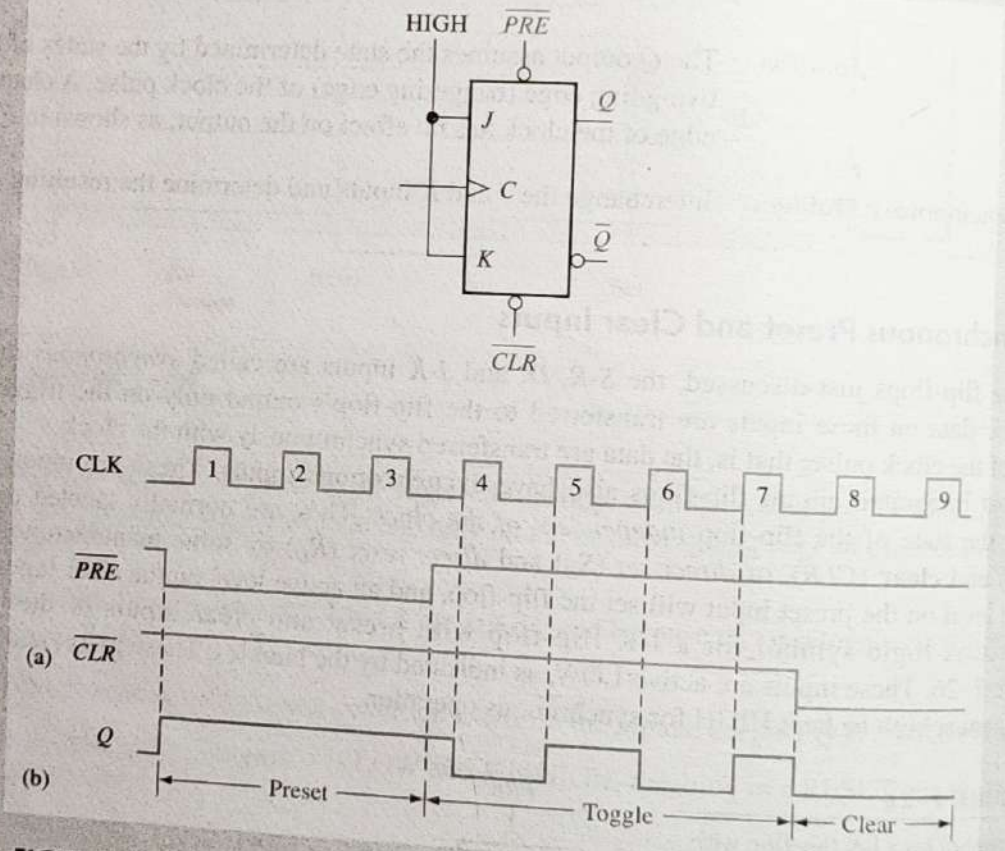


FIGURE 7–28

Solution **1.** During clock pulses 1, 2, and 3, the preset ($\overline{PRE}$) is LOW, keeping the flip-flop SET regardless of the synchronous *J* and *K* inputs.

2. For clock pulses 4, 5, 6, and 7, toggle operation occurs because J is HIGH, K is HIGH, and both $\overline{PRE}$ and $\overline{CLR}$ are HIGH.
3. For clock pulses 8 and 9, the clear ($\overline{CLR}$) input is LOW, keeping the flip-flop RESET regardless of the synchronous inputs.

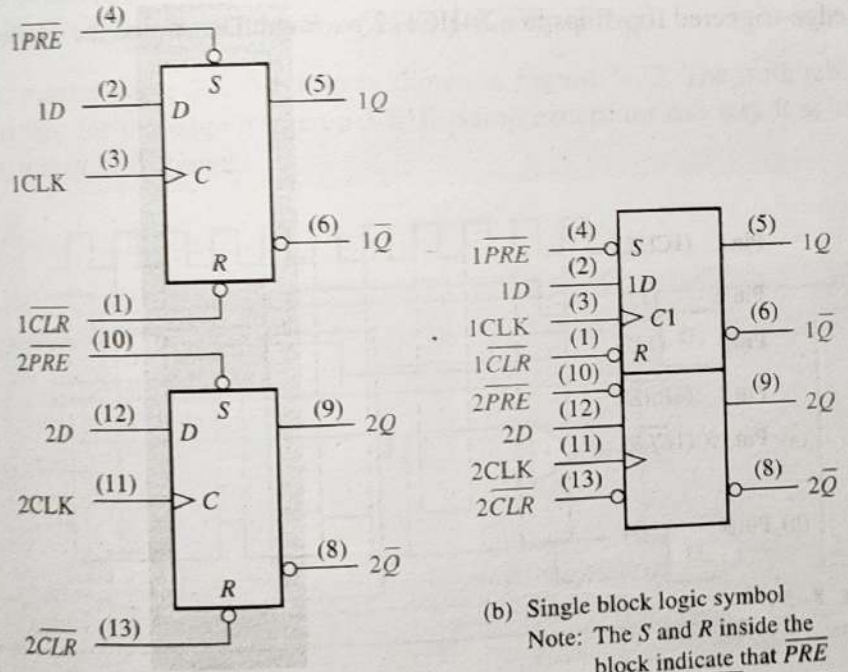
The resulting Q output is shown in Figure 7–28(b).

Supplementary Problem If you interchange the $\overline{PRE}$ and $\overline{CLR}$ waveforms in Figure 7–28(a), what will the Q output look like?

FLIP-FLOPS

Let us look at two specific edge-triggered flip-flops. They are representative of the various types of flip-flops available in IC form and, like most other devices, are available in CMOS and in TTL.

74AHC74 Dual D Flip-Flops This CMOS device contains two identical flip-flops that are independent of each other except for sharing V_{CC} and ground. The flip-flops are positive edge-triggered and have active-LOW asynchronous preset and clear inputs. The logic symbols for the individual flip-flops within the package are shown in Figure 7–29(a), and an ANSI/IEEE standard single block symbol that represents the entire device is shown in part (b). The pin numbers are shown in parentheses.



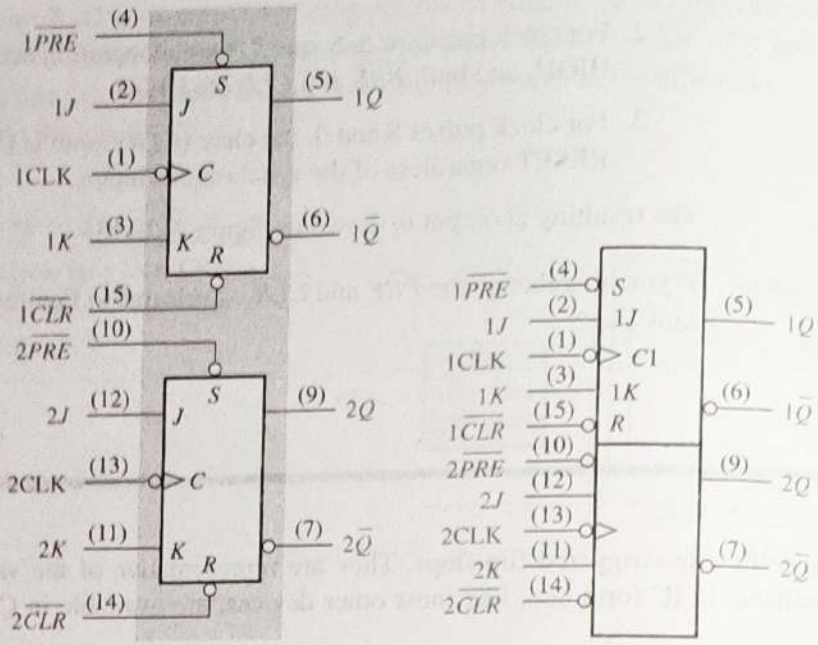
(a) Individual logic symbols

(b) Single block logic symbol
Note: The S and R inside the block indicate that $\overline{PRE}$ SETS and $\overline{CLR}$ RESETS

FIGURE 7–29

74HC112 Dual J-K Flip-Flops This CMOS device also has two identical flip-flops that are negative edge-triggered and have active-LOW asynchronous preset and clear inputs. The logic symbols are shown in Figure 7–30.

FIGURE 7–30



(a) Individual logic symbols (b) Single block logic symbol

EXAMPLE 7–9

The 1*J*, 1*K*, 1CLK, $1\overline{PRE}$, and $1\overline{CLR}$ waveforms in Figure 7–31(a) are applied to one of the negative edge-triggered flip-flops in a 74HC112 package. Determine the 1*Q* output waveform.

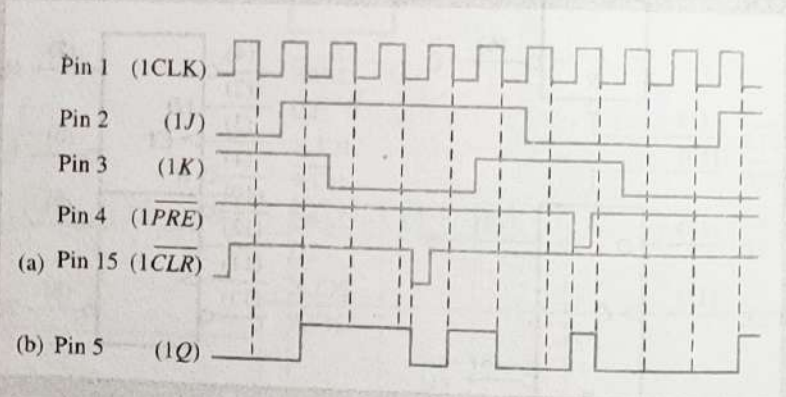


FIGURE 7–31

Solution The resulting 1*Q* waveform is shown in Figure 7–31(b). Notice that each time a LOW is applied to the $1\overline{PRE}$ or $1\overline{CLR}$, the flip-flop is set or reset regardless of the states of the other inputs.

Supplementary Problem Determine the 1*Q* output waveform if the waveforms for $1\overline{PRE}$ and $1\overline{CLR}$ are inter-changed.

SECTION 7–2 REVIEW

1. Describe the main difference between a gated S-R latch and an edge-triggered S-R flip-flop.
2. How does a J-K flip-flop differ from an S-R flip-flop in its basic operation?
3. Assume that the flip-flop fin Figure 7–21 is negative edge-triggered. Describe the output waveform for the same CLK and *D* waveforms.

7–3 MASTER-SLAVE FLIP-FLOPS

Another class of flip-flop is the pulse-triggered master-slave, which has largely been replaced by the edge-triggered devices. Although master-slave flip-flops are essentially becoming obsolete, you may encounter this type of flip-flop in some existing equipment. Data are entered into the flip-flop at the leading edge of the clock pulses, but the output does not reflect the input state until the trailing edge. The pulse-triggered master-slave flip-flop does not allow data to change while the clock pulse is active.

After completing this section, you should be able to

- Identify a master-slave flip-flop by its logic symbol
- Explain how the master-slave flip-flop differs from the edge-triggered devices
- Discuss the basic operation of the pulse-triggered master-slave flip-flop

The Pulse-Triggered Master-Slave J-K Flip-Flop

A basic **master-slave** J-K flip-flop is shown in Figure 7–32. The truth table operation is the same as that for the edge-triggered J-K flip-flop except for the way it is clocked. Internally, though, it is quite different.

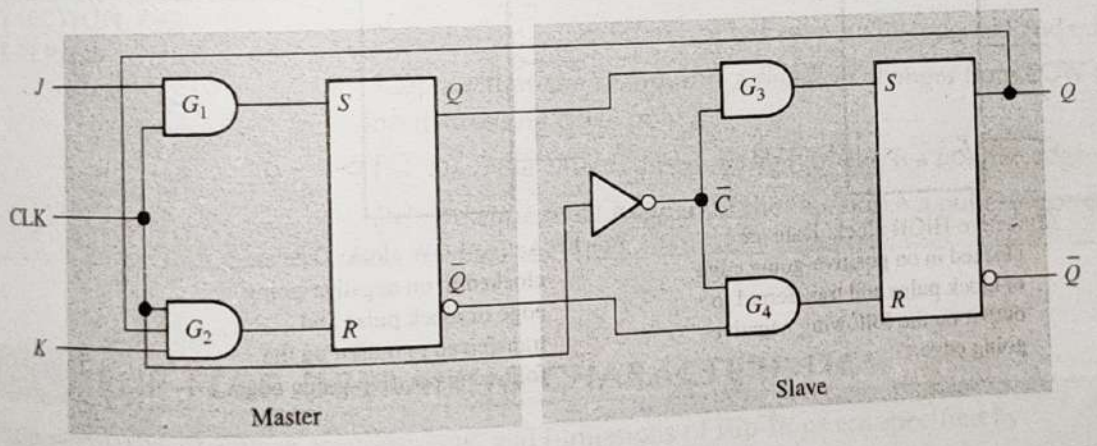


FIGURE 7–32
Basic logic diagram for a master-slave J-K flip-flop

This type of flip-flop is composed of two sections, the master section and the slave section. The master section is basically a gated latch, and the slave section is the same except that it is clocked on the inverted clock pulse and is controlled by the outputs of the master section rather than by the external *J-K* inputs.

The master section will assume the state determined by the J and K inputs beginning at the leading (positive-going) edge of the clock pulse. The state of the master section is then transferred to the slave section on the trailing edge of the clock pulse because the outputs of the master are applied to the inputs of the slave and the clock pulse to the slave is inverted. At the trailing edge of the clock pulse, the state of the slave then appears on the Q and $\overline{Q}$ outputs. The Q output is connected back to an input of gate G_2 and the $\overline{Q}$ output is connected back to an input of gate G_1 to produce the characteristic toggle operation when $J = 1$ and $K = 1$. The logic operation is summarized in Table 7–5. One limitation to master-slave operation is that the inputs (J and K) cannot change while the clock pulse is active because the state of the master latch can change during this time.

TABLE 7–5

Truth table for the master-slave J-K flip-flop

INPUTS			OUTPUTS		
J	K	CLK	Q	$\overline{Q}$	COMMENTS
0	0	⊓	Q_0	$\overline{Q}_0$	No change
0	1	⊓	0	1	RESET
1	0	⊓	1	0	SET
1	1	⊓	$\overline{Q}_0$	Q_0	Toggle

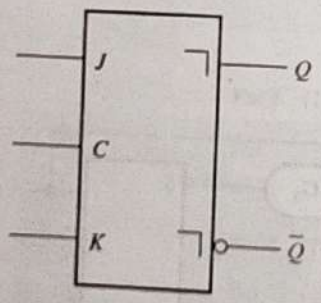
⊓ = clock pulse

Q_0 = output level before clock pulse

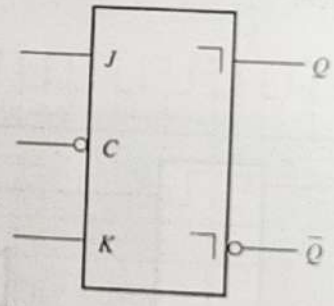
The logic symbols for the J-K master-slave flip-flop are shown in Figure 7–33. The key to identifying a pulse-triggered (master-slave) flip-flop by its logic symbol is the ANSI/IEEE *postponed output* symbol (⌝) at the outputs. This symbol means that the output does not reflect the J-K input data until the occurrence of the clock edge (either positive-going or negative-going) following the triggering edge. Notice that there is no dynamic input indicator (▷) at the clock (C) input as there is for an edge-triggered flip-flop.

FIGURE 7–33

Pulse-triggered (master-slave) J-K flip-flop logic symbols



(a) Active-HIGH clock: Data are clocked in on positive-going edge of clock pulse and transferred to output on the following negative-going edge.

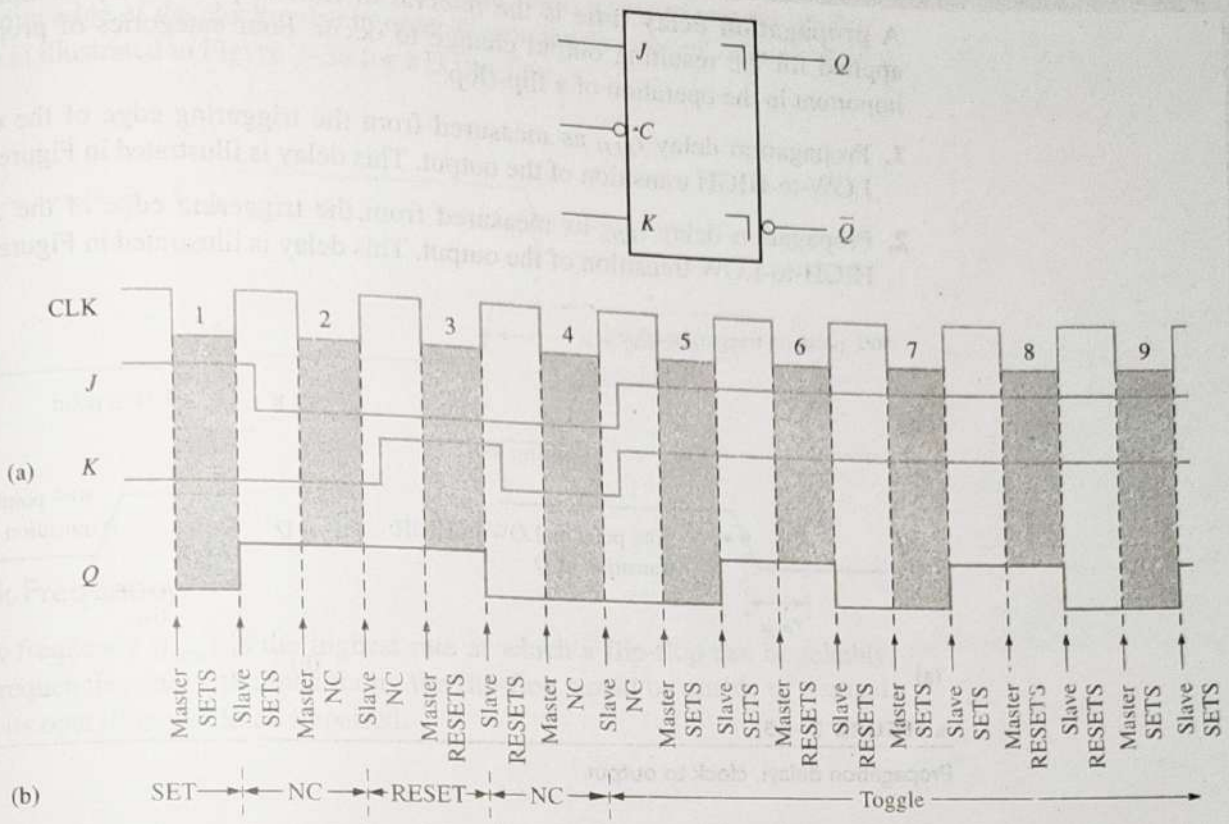


(b) Active-LOW clock: Data are clocked in on negative-going edge of clock pulse and transferred to output on the following positive-going edge.

EXAMPLE 7–10

Determine the Q output of the master-slave J-K flip-flop for the input waveforms shown in Figure 7–34(a). The flip-flop starts out RESET and the clock is active-LOW.

Solution The Q waveform is shown in Figure 7–34(b). The input states and events at the beginning and end of each clock pulse are labelled to demonstrate the operation. NC means no change.



▲ FIGURE 7–34

Supplementary Problem What would the Q output look like if the J and K waveforms were inverted?

SECTION 7–3 REVIEW

1. Describe the basic difference between pulse-triggered and edge-triggered flip-flops.
2. Suppose that the D input of a flip-flop changes from LOW to HIGH in the middle of a positive-going clock pulse.
   (a) Describe what happens if the flip-flop is a positive edge-triggered type.
   (b) Describe what happens if the flip-flop is a pulse-triggered master-slave type.

7–4 FLIP-FLOP OPERATING CHARACTERISTICS

The performance, operating requirements, and limitations of flip-flops are specified by several operating characteristics or parameters found on the data sheet for the device. Generally, the specifications are applicable to all CMOS and TTL flip-flops.

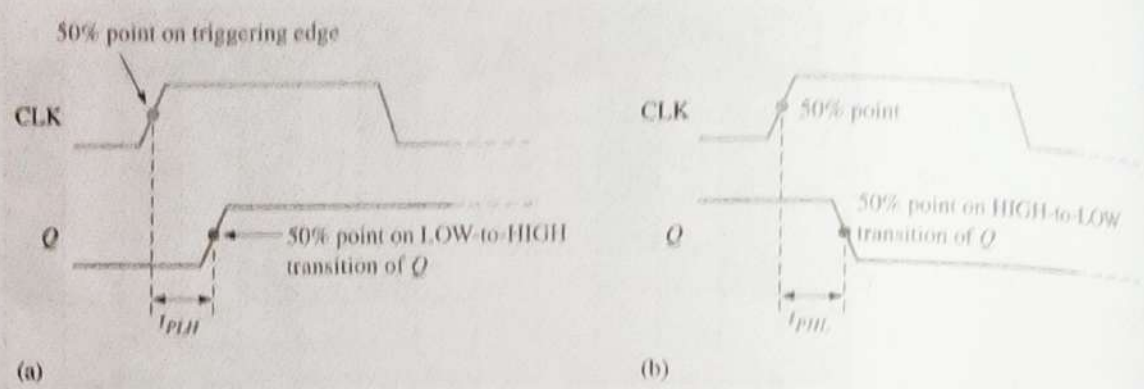
After completing this section, you should be able to

■ Define *propagation delay time* ■ Explain the various propagation delay time specifications ■ Define *hold time* and discuss how it limits flip-flop operation ■ Define *set-up time* and discuss how it limits flip-flop operation ■ Discuss the significance of maximum clock frequency ■ Discuss the various pulse width specifications ■ Define *power dissipation* and calculate its value for a specific device ■ Compare various series of flip-flops in terms of their operating parameters

Propagation Delay Times

A **propagation delay time** is the interval of time required after an input signal has been applied for the resulting output change to occur. Four categories of propagation delay are important in the operation of a flip-flop:

1. Propagation delay t_{PLH} as measured from the triggering edge of the clock pulse to the LOW-to-HIGH transition of the output. This delay is illustrated in Figure 7–35(a).
2. Propagation delay t_{PHL} as measured from the triggering edge of the clock pulse to the HIGH-to-LOW transition of the output. This delay is illustrated in Figure 7–35(b).

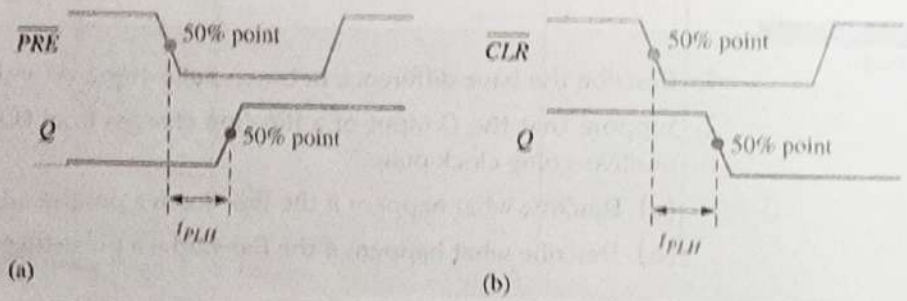


▲ FIGURE 7–35

Propagation delays, clock to output

3. Propagation delay t_{PLH} as measured from the leading edge of the preset input to the LOW-to-HIGH transition of the output. This delay is illustrated in Figure 7–36(a) for an active-LOW preset input.
4. Propagation delay t_{PHL} as measured from the leading edge of the clear input to the HIGH-to-LOW transition of the output. This delay is illustrated in Figure 7–36(b) for an active-LOW clear input.

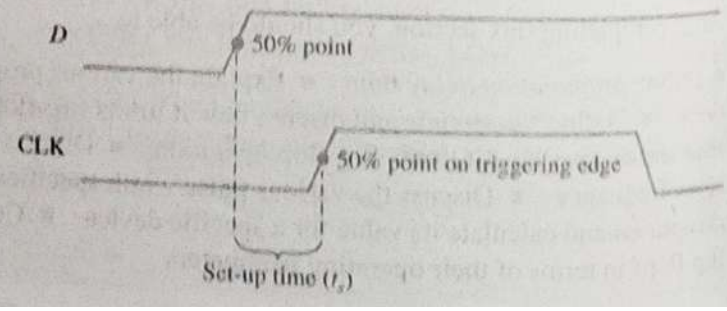
▶ FIGURE 7–36



Set-up Time

The **set-up time** (t_s) is the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or S and R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. This interval is illustrated in Figure 7–37 for a D flip-flop.

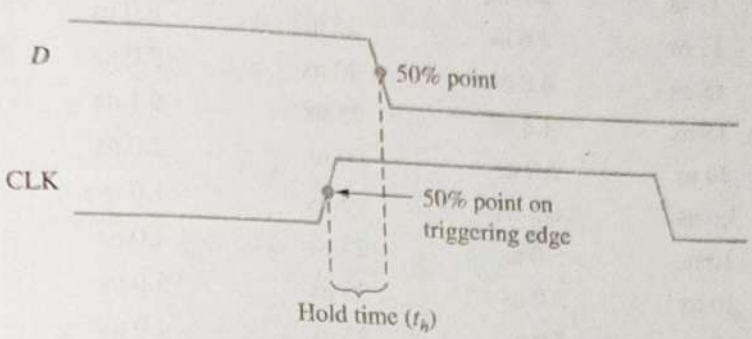
▶ FIGURE 7–37



Hold time

The **hold time** (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. This is illustrated in Figure 7–38 for a D flip-flop.

FIGURE 7–38



Maximum Clock Frequency

The maximum clock frequency (f_{max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The power **dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} \times I_{CC} = 5\text{ V} \times 5\text{ mA} = 25\text{ mW}$$

The power dissipation is very important in most applications in which the capacity of the dc supply is a concern. As an example, let us assume that you have a digital system that requires a total of ten flip-flops, and each flip-flop dissipates 25 mW of power. The total power requirement is

$$P_T = 10 \times 25\text{ mW} = 250\text{ mW} = 0.25\text{ W}$$

This tells you the output capacity required of the dc supply. If the flip-flops operate on +5 V dc, then the amount of current that the supply must provide is

$$I = \frac{250\text{ mW}}{5\text{ V}} = 50\text{ mA}$$

You must use a +5 V dc supply that is capable of providing at least 50 mA of current.

Comparison of Specific Flip-flops

Table 7–6 provides a comparison, in terms of the operating parameters discussed in this section, of four CMOS and TTL flip-flops of the same type.